UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LEI CHENG

Appeal 2007-0959
Application 10/082,893
Technology Center 2100

Decided: May 7, 2007

Before KENNETH W. HAIRSTON, ALLEN R. MACDONALD, and JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-30, the only claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

STATEMENT OF THE CASE

Appellant invented a method and system for transferring data from a host memory to an Ethernet device. Specifically, data is transferred directly to the Ethernet device without storing the data in the embedded memory of an adapter that includes the Ethernet device. Such a technique improves transmit performance by eliminating the need to copy the data to the embedded memory.[1] Claim 1 is illustrative:

> 1. A method comprising:
> transferring data from a host memory to an Ethernet device; and
> processing the data without sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device.

The Examiner relies on the following prior art reference to show unpatentability:

Davis	US 6,324,609 B1	Nov. 27, 2001

The Examiner's rejection is as follows:

Claims 1-30 are rejected under 35 U.S.C. § 102(e) as being anticipated by Davis.

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Briefs and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellant. Arguments which Appellant could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

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[1] *See generally* Specification 7:19 - 8:2.

The Examiner has indicated how the claimed invention is deemed to be fully met by the disclosure of Davis (Answer 3-4). Regarding independent claim 1, Appellant argues that Davis does not disclose: (1) transferring data from a host memory; (2) an Ethernet device; and (3) processing data without sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device as claimed (Br. 11-12). Appellant emphasizes that Davis' system uses a configuration cycle to identify peripheral devices, but no data is transferred to them (Br. 11). Appellant adds that nothing in Davis teaches how information would be transferred to an Ethernet device without using the embedded memory associated with an adapter that includes the Ethernet device (Br. 12; Reply Br. 2).

The Examiner argues that Davis discloses transferring data from a host memory as claimed since the host processor sends Type 1 commands to the bridge to determine all devices connected to the PCI bus so that drivers can be loaded to these devices (Answer 4-5). The Examiner also contends that the PCI devices connected to the PCI bus 15 in Davis are "equivalent" to those disclosed in Appellant's Specification (Answer 5). The Examiner also argues that the features upon which Appellant's arguments rely (i.e., with respect to not transferring data to the adapter's embedded memory) are not recited in the claims (Answer 6).

For the reasons that follow, we affirm.

ISSUE

Has Appellant established that the Examiner erred in finding that the disclosure of Davis anticipates the claims?

FINDINGS OF FACT

Davis discloses a computer system comprising a host processor 3 that communicates with I/O processor 5 via primary PCI bus 7. The I/O processor communicates with the PCI devices 9, 11, and 13 via secondary PCI bus 15 (Davis, col. 6, ll. 53-58; Fig. 1). PCI device 11 can be an Ethernet network controller (Davis, col. 7, ll. 4-5). Both the host processor and I/O processor contain memories (Davis, col. 6, ll. 64-67; col. 7, ll. 7-59; Fig. 2). Additionally, host processor can configure any public devices on secondary PCI bus 15 (Davis, col. 14, ll. 24-26).

In one embodiment, private PCI devices can be established. To this end, Type 1 commands[2] received by the primary PCI interface 33 of bridge 29 are converted to Type 0 commands by bridge 20 to configure PCI devices connected to secondary PCI interface 35 (Davis, col. 7, ll. 60-67; col. 14, l. 27 - col. 15, l. 25).

PRINCIPLES OF LAW

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Applied Digital Data Systems, Inc.*, 730 F.2d 1440, 1444, 221 USPQ 385,

[2] A "Type 1" command is used to pass a configuration request to a target device on a bus other than the bus where a specific transaction is being run. A "Type 0" command, however, is used to select a device on the bus where the transaction is being run and is not propagated beyond the local PCI bus. *See generally* PCI Local Bus Specification, Rev. 2.2, at 31.

388 (Fed. Cir. 1984); *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983).

ANALYSIS

At the outset, we note that the second limitation recited in independent claim 1, namely "processing the data *without* sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device" essentially recites a negative limitation. That is, the scope and breadth of claim 1 is fully met by a method that includes processing the data transferred from the host memory to an Ethernet device if the method does not otherwise disclose the negative limitation -- namely sending the data to an Ethernet adapter's embedded memory.

With this interpretation, we turn to Davis. First, contrary to Appellant's argument, Davis does in fact disclose an Ethernet device: PCI device 11 can be an Ethernet network controller (Davis, col. 7, ll. 4-5).[3]

In Davis, host processor 3 communicates with I/O processor 5 via primary PCI bus 7. The I/O processor in turn communicates with the PCI

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[3] Although the Examiner cites an additional non-patent document to show that a PCI device can be an Ethernet device (Answer 5), this additional reference was not relied upon in the rejection and is not therefore before us. *See In re Hoch*, 428, F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970) ("Where a reference is relied on to support a rejection, whether or not in a 'minor capacity,' there would appear to be no excuse for not positively including the reference in the statement of the rejection.").

Moreover, the Examiner's reference to this document to show that PCI devices *can be* (but not necessarily are) Ethernet devices is not germane to anticipation, but rather obviousness--an issue not before us on appeal. In any event, this issue is moot since Davis expressly discloses Ethernet devices as we indicate in our opinion.

devices 9, 11, and 13 via secondary PCI bus 15 (Davis, col. 6, ll. 53-58). Such data communication with the Ethernet device 11 certainly involves transferring data to the Ethernet device as well as to the other PCI devices via the primary and secondary PCI buses. Although we find the Examiner's assertion that drivers are loaded to the PCI devices problematic essentially for the reasons noted by Appellant, the PCI devices are nonetheless in data communication with the processors via the respective PCI buses.

We further note that the scope and breadth of the term "host memory" does not preclude either the host processor 3 or the I/O processor 5 -- processors that each contain memory.[4] Both processors communicate with -- and therefore transfer data to -- the Ethernet device.

Significantly, Davis is silent whether such processed data transferred to the Ethernet device noted above is or is not sent to an embedded memory associated with an adapter that includes the Ethernet device. Indeed, Davis is silent regarding whether the Ethernet device is associated with an adapter at all, let alone whether data is sent to an embedded memory associated with such an adapter. Such silence, however, fully meets the negative limitation recited in claim 1 given the scope and breadth of the limitation.

In short, Appellant has simply not persuasively rebutted the Examiner's prima facie case of anticipation based on the disclosure of Davis. In this regard, Appellant has provided no evidence on this record to show that (1) the Ethernet device in Davis necessarily is included within an adapter associated with an embedded memory, and (2) the processed data

[4] *See* Davis, at col. 6, ll. 64-67 (noting that host processor 3 can contain main and cache memories); *see also* Davis, at col. 7, ll. 7-59 and Fig. 2 (detailing I/O processor 5).

transferred to Davis' Ethernet device is necessarily sent to this embedded memory.

For at least these reasons, Davis fully meets independent claim 1. Since Appellant has not separately argued the patentability of claims 2-30 with particularity, these claims fall with independent claim 1. *See In re Nielson*, 816 F.2d 1567, 1572, 2 USPQ2d 1525, 1528 (Fed. Cir. 1987); *see also* 37 C.F.R. § 41.37(c)(1)(vii).

CONCLUSION OF LAW

On the record before us, Appellant has not established that the Examiner erred in finding that the disclosure of Davis anticipates the claims.

DECISION

We have sustained the Examiner's rejection with respect to all claims on appeal. Therefore, the Examiner's decision rejecting claims 1-30 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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